	Application No.	Applicant(s)
Notice of Allowability	09/815,772	CHAN, JOHNI
	Examiner	Art Unit
	Donna K. Mason	2111
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to <u>Paper filed on March 8, 2005</u> .		
2. The allowed claim(s) is/are 1.3 and 5-18 (renumbered 1-16).		
3. The drawings filed on <u>25 March 2002</u> are accepted by the Examiner.		
4.		
Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. Interview Summary Paper No./Mail Date Pape	e

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DETAILED ACTION

Allowable Subject Matter

- 1. Claims 1, 3 and 5-18 are allowed.
- 2. The following is an examiner's statement of reasons for allowance:

Regarding claims 1, 3 and 5, the primary reason for allowance is the inclusion of the limitation, "wherein the first hybrid switching module further comprises a failure mode that couples the first input/output link data channel with the first main bus when the first processor fails allowing the second processor to access the first peripheral device on the first main bus to implement the first function, and the second hybrid switching module further comprises a failure mode that couples the second input/output link data channel with the second main bus when the second processor fails allowing the first processor to access the second peripheral device on the second main bus to implement the second non-redundant function," as recited in independent claim 1.

The prior art is not directed to a system, as claimed, having a failure mode that couples input/output link data channels in the manner claimed. For example, U.S. Patent No. 4,968,977 to Chinnaswamy et al. ("Chinnaswamy") does not expressly disclose coupling the input/output link data channels in the event of processor failure, but rather teaches the use of a second hybrid switching module for expansion purposes only. By way of further example, although U.S. Patent No. 4,014,005 to Fox, et al. ("Fox") does teach a failure mode, this patent does not expressly disclose coupling the input/output link data channels upon processor failure, in the manner claimed.

recited in independent claim 13.

Regarding claims 6-18, the primary reason for allowance is the inclusion of the limitation, "wherein the first switch selectively couples to the first bridge and selectively couples to the input/output link data channel, wherein the first hybrid switching module processor data channel is thereby selectively coupled to the first bridge allowing access over a first main bus to a first peripheral device that implements a first function, and selectively coupled to the input/output link data channel allowing access over a second

main bus to a second peripheral device that implements a second function that is not

redundant to the first function," as recited in independent claim 6, and as similarly

The prior art is not directed to an apparatus, as claimed, where the first switch selectively couples to the input/output link data channel, in the manner claimed. For example, Chinnaswamy discloses a first hybrid switching module (Fig. 2, item 32; and Fig. 3, item 32) and a second hybrid switching module (Fig. 2, item 34), where the first hybrid switching module has a first input/output link data channel and the second hybrid switching modules has a second input/output link data channel (Fig. 2, EXP. PORT 1 (IN and OUT) and EXP. PORT 2 (IN and OUT)). As shown in Fig. 3, Chinnaswamy also discloses a first switch (DEMUX 1) that selectively couples to the first bridge (Fig. 3, MUX 4) and selectively couples to the *output* link data channel (Fig. 3, OUTPUT EXPANSION PORT). In this way, Chinnaswamy does not expressly disclose selectively coupling to the *input* link data channel (Fig. 3, INPUT EXPANSION PORT), which forms part of the input/output link data channel.

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By way of further example, Fox does not expressly disclose where the first switch (Fig. 1, CROSS-BAR SW 1) selectively couples to the first bridge (Fig. 5, DECODER SECTION), or where the first switch selectively couples to the input/output link data channel (see channel connecting CROSS-BAR SW 1 and CROSS-BAR SW M). To the

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contrary, Fox discloses where the switch is always connected to the bridge. Also, the data channels connecting the first and second hybrid switching modules are input lines only, which provide inputs from the processors to the hybrid switching modules.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (571) 272-3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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DKM

MARK H. RINEHART SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2100